Amendments to the Specification:

Please amend the **Summary of the Invention** as follows:

Summary of the Invention

The present invention is directed to a silicon-on-insulator integrated circuit that comprises a handle die, a substantially continuous and unbroken silicide layer over the handle die, and a substantially continuous and unbroken first dielectric layer overlying one side of the silicide layer. A device silicon layer having an upper surface overlies the first dielectric layer, and a second dielectric layer on the handle die underlies the opposite side of the silicide layer. Interconnected transistors are disposed in and at the upper surface of the device silicon layer.

Also in accordance with the present invention is a silicon-on-insulator integrated circuit that includes a handle die and a first dielectric layer formed on the handle die. A substantially continuous and unbroken silicide layer is formed on the first dielectric layer; the silicide layer has a controlled resistance and provides a diffusion barrier to impurities. A substantially continuous and unbroken second dielectric layer is disposed between the silicide layer and a device silicon layer, and trenches extend through the device silicon layer and silicon layer and separate the device silicon layer into islands, each having an underlying continuous silicide area. Interconnected transistors are disposed in and at an upper surface of the device silicon layer.

The present invention is further directed to a bonded wafer integrated circuit that comprises a handle die and a homogeneous silicide layer bonded to the handle die. A device layer is bonded to the silicide layer, and interconnected transistors are disposed in and at a surface of device layer. ~~The silicide layer comprises bonding material that differs from material in the portion of the handle die adjacent the silicide layer and also differs from material in the portion of the device layer adjacent the silicide layer.~~

The present invention provides silicon-on-insulator bonded wafer processing with the features of (1) relatively low temperature bonding by the use of low temperature, about 500-800° C metal silicidation reactions for bonding; (2) better stress compensation

by providing materials in the bonding zone that will produce silicides with coefficients of thermal expansion closely matched to those of the substrate wafers and buried dielectric layers, thereby reducing warpage; (3) limiting contaminant migration by means of a bonding zone that provides a barrier to diffusion of mobile contaminants; (4) simultaneously producing a buried doped layer in the silicon during the bonding process; (5) a conductive, dielectrically-isolated layer at the bonding zone; and (6) a thermally conductive layer at the bonding zone.

Please amend the **Abstract** as follows:

A silicon-on-insulator integrated circuit comprises a handle die, a substantially continuous and unbroken silicide layer over the handle die, and a substantially continuous and unbroken first dielectric layer overlying one side of the silicide layer. A device silicon layer having an upper surface overlies the first dielectric layer, and a second dielectric layer on the handle die underlies the opposite side of the silicide layer. Interconnected transistors are disposed in and at the upper surface of the device silicon layer. A silicon-on insulator integrated circuit includes a handle die and a first dielectric layer formed on the handle die. A substantially continuous and unbroken silicide layer is formed on the first dielectric layer; the silicide layer has a controlled resistance and provides a diffusion barrier to impurities. A substantially continuous and unbroken second dielectric layer is disposed between the silicide layer and a device silicon layer, and trenches extend through the device silicon layer and silicide layer and separate the device silicon layer into islands, each having an underlying continuous silicide area. Interconnected transistors are disposed in and at an upper surface of the device silicon layer. A bonded wafer integrated circuit comprised a handle die and a homogeneous silicide layer bonded to the handle die. A device layer is bonded to the silicide layer, and interconnected transistors are disposed in and at a surface of device layer. ~~The silicide layer comprises bonding material that differs from material in the portion of the handle~~

~~die adjacent the silicide layer and also differs from material in the portion of the device layer adjacent the silicide layer.~~